## What is claimed is:

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1. A voltage-level comprising:

a static voltage-level converter; and

a split-level output dircuit coupled to the static voltage-level converter.

1 2. The voltage-level converter of claim 1, wherein the static voltage-level converter comprises:

an input node, a first output node, and a second output node;

a first pair of transistors connected in series, the first pair of transistors including a first transistor and a second transistor, the first transistor coupled to the input node;

a second pair of transistors connected in series, the second pair of transistors including a first transistor and a second transistor, the second transistor of the second pair of transistors being cross-coupled with the second transistor of the first pair of transistors and the second transistor of the second pair of transistors being coupled to the first output node; and

an inverter coupled to the input node, to the first transistor of the second pair of transistors, and to the second output node.

- 1 3. The voltage level converter of claim 2, wherein the split-level output circuit comprises a plurality of insulated-gate field-effect transistors.
- 1 4. The voltage-level converter of claim 1, wherein the static voltage-level converter
- 2 comprises a first output node and a second output node and the split-level output circuit
- 3 comprises a first split-level input node, a second split-level input node, a split-level
- output node, a first insulated-gate field-effect transistor (FET) coupled to the first split-
- 5 level input node and a second insulated-gate FET coupled to the second split-level input
- 6 node, the first insulated-gate FET being connected in series with the second insulated-
- 7 gate FET, the first insulated gate FET and the second insulated gate FET having a

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- 8 common node coupled to the split-level output node and the first split-level input node
- 9 coupled to the first output node and the second split-level input node coupled to the
- 10 second output node.
- 1 5. The voltage-level converter of claim 4, wherein the first insulated-gate field-effect
- 2 transistor comprises a p-type insulated-gate field-effect transistor.
- 1 6. The voltage-level converter of claim 5, wherein the second insulated-gate field-
- 2 effect transistor comprises an n-type insulated gate field-effect transistor.
- 1 7. A voltage-level converter comprising:
- a static voltage-level converter including an input node, a first pull-up node, a
- 3 second pull-up node, an inverter output node, and an output node;
- a first transistor coupled to the input node and the first pull-up node; and
- a second transistor coupled to the second pull-up node and the inverter output
- 6 node.
- 1 8. The voltage-level converter of claim 7, wherein the first transistor comprises an
- 2 insulated gate field-effect transistor and the second transistor comprises an insulated-gate
- 3 field-effect transistor.
- 1 9. The voltage-level converter of claim 7, wherein the first transistor comprises a p-
- 2 type insulated-gate field-effect transistor and the second transistor comprises a p-type
- 3 insulated-gate field-effect transistor.
- 1 10. The voltage-level converter of claim 9, further comprising:
- 2 an inverter coupled to the output node.

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input inverter.

The voltage-level converter of claim 10, wherein the inverter comprises: 1 11. 2 a single-input inverter. The voltage-level converter of claim 11, wherein the inverter comprises: 1 12. an n-type insulated-gate field-effect transistor coupled to the output node; 2 a first p-type insulated-gate field-effect transistor coupled to the inverter output 3 4 node; a second p-type insulated-gate field-effect transisfor coupled to the static level 5 converter, wherein the n-type insulated-gate field-effect/transistor, the first p-type 6 7 insulated-gate field-effect transistor, and the second p-type insulated-gate field-effect 8 transistor are connected in series. 1 13. A voltage-level converter comprising: 2 a static voltage-level converter having an input node and an output node; 3 a first transistor coupled to the input node and the static voltage-level converter; 4 and 5 a second transistor coupled to the static voltage-level converter. The voltage-level converter of claim 1/3, wherein the first transistor comprises a p-1 14. 2 type insulated-gate field-effect transistor. The voltage-level converter of claim 14, wherein the second transistor comprises a 1 15. 2 p-type insulated-gate field-effect transistor The voltage-level converter of claim 15, further comprising: 1 16. an inverter coupled to the output node. 2 1 17. The voltage-level converter of claim 16, wherein the inverter comprises a single-

1	18.	The voltage-level converter of claim 16, wherein the inverter comprises:
2		a multiple-input inverter coupled to at least three outputs of the static voltage-
3	level c	onverter.
1	19.	A voltage-level converter comprising:
2		a static voltage-level converter comprising an input node, an output node, a first
3	pair of	serially connected transistors, a second pair of serially connected transistors, and
4	an inv	erter coupled between the first pair of serially connected transistors and the second
5	pair of	Serially connected transistors;
6		a first transistor located between the first pair of serially connected transistors and
7	couple	ed to the input node; and
8		a second transistor located between the second pair of serially connected
9	transis	tors and coupled to the inverter.
1	20.	The voltage-level converter of claim 19, wherein the first transistor comprises an
2	insulat	ted-gate field-effect transistor.
1	21.	The voltage-level converter of claim 20, wherein the second transistor comprises
2	an inst	ulated-gate field-effect transistor.
1	22.	The voltage-level converter of claim 21, further comprising:
2		a buffer coupled to the output node.
1	23.	The voltage-level converter of claim 22, wherein the buffer comprises a single-
2	innut i	nverter

1	24. The voltage-level converter of claim 22, wherein the buffer comprises:	
2	a multiple-input inverter coupled to at least three outputs of the static vo	ltage-
3	level converter.	
1	25. The voltage-level converter of claim 24, wherein the multiple-input inve	rter has
2	an inverter output node and comprises:	
3	an n-type insulated-gate field-effect transistor;	
4	a first p-type insulated-gate field-effect transistor; and	
5	a second p-type insulated-gate field-effect transistor, wherein the n-type	insulated-
6	gate field-effect transistor, the first p-type insulated gate field-effect transistor,	and the
7	second p-type insulated-gate field-effect are connected in series and the n-type in	nsulated-
8	gate field-effect transistor is coupled to the inverter output node, the first p-type	;
9	insulated-gate field-effect transistor is coupled to the first pair of serially connection	eted
10	transistors, and the second p-type insulated-gate field-effect transistor is coupled to the	
11	inverter output node.	
1	26. A logic unit comprising:	
2	one or more first logic units adapted to operate at a first voltage;	
3	one or more second logic units adapted to operate at a second voltage, the	ne second
4	voltage being greater than the first/voltage; and	
5	a voltage-level converter for coupling at least one of the one or more fir	st logic
6	units to at least one of the one or more second logic units, the voltage-level con	verter
7	comprising:	
8	a first voltage-level converter comprising an input node coupled	to the at
9	least one of the one or more first logic units, an output node coupled to	he at least
10	one of the one or more second logic units, an inverter output node, a first	t pair of
11	serially connected transistors, and a second pair of serially connected transitions.	ınsistors;
12	and f	
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13	a first transistor located between the first pair of serially connected
14	transistors and coupled to the input node; and
15	a second transistor located between the second pair of serially connected
16	transistors and coupled to the inverter output node.
1	27. The voltage-level converter of claim 26, wherein the first transistor comprises a
2	first insulated-gate field-effect transistor and the second transistor comprises a second
3	insulated-gate field-effect transistor.
1	28. The voltage-level converter of claim 27, wherein the first insulated-gate field-
2	effect transistor comprises a p-type insulated-gate field-effect transistor and the second
3	insulated-gate field-effect transistor comprises a p-type insulated-gate field-effect
4	transistor.
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